AGP Inline Memory Module

Specification

April 2000

Order Number: 298177-004

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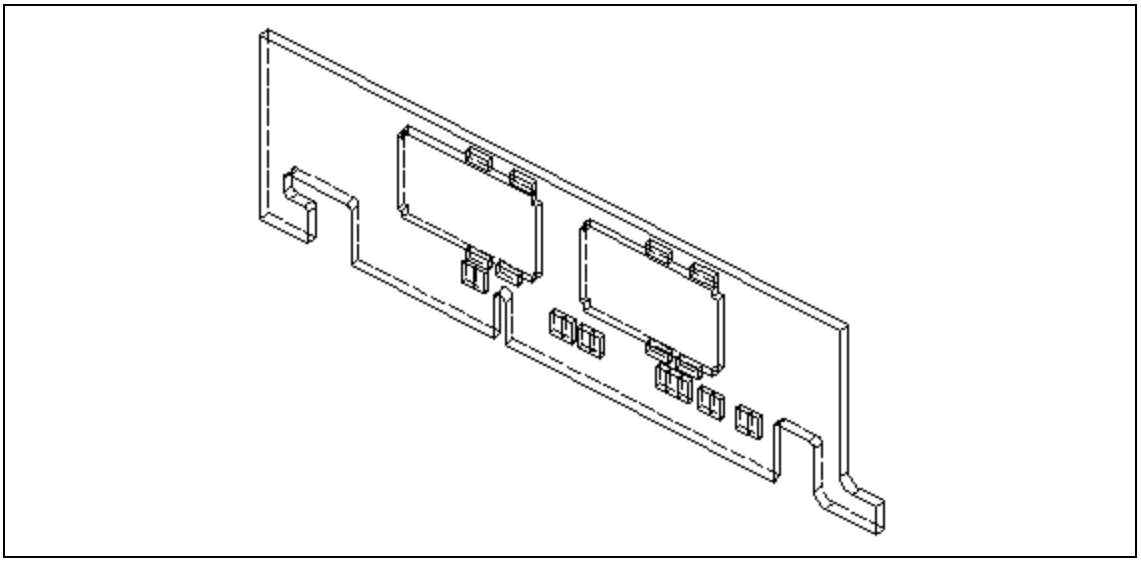
Revision History

Rev	Draft/Changes	Date
-001	Initial release (Spec revision 0.8)	December 1999
-002	Added section 3 on memory component specification (Spec revision 0.81)	January 2000
-003	Revised schematics and BOM, added various clarifications. (Spec revision 0.9)	March 2000
-004	Updated Mechancial Design and Layout to include new silk screen (Spec revision 1.0)	April 2000

1. Introduction

This specification specifies electrical and mechanical characteristics of an AGP Inline Memory Module (AIMM). The AIMM is intended for use as a local memory subsystem for a graphics core integrated in a core-logic chipset. These AIMMs are intended to provide 4 MB of addressable SDRAM (arranged as 1Mx32), which resides on a module in a 3.3V or universal AGP slot.



Two local memory configurations are currently defined for AIMMs. Two 1Mx16 SDRAM devices may be used or a single 2Mx32 SDRAM device may be used (only 1Mx32 of which is addressable). Schematics for both implementations are included in this specification.

The AIMM is designed to operate with a 32-bit wide SDRAM controller running at 133 MHz. The components populating the AIMM must meet the *Intel PC SGRAM/SDRAM Specification for Graphics* Version 0.99 requirements for 133 MHz parts. AIMM modules must use SDRAM components with 3-3-3 timings at a minimum.

This specification focuses on AIMM implementations using 1Mx16 or 2Mx32 SDRAM on a 4-layer single-sided assembly PCB.

Related Documents

- *Intel PC SGRAM/SDRAM Specification for Graphics* Version .99 (Q1 1999)
- *Accelerated Graphics Port Interface Specification* - http://www.intel.com/technology/agp/agp_index.htm

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2. Environmental Requirements

The AIMM designs operate within a personal computer cabinet in an office environment with limited capacity for heating and air conditioning. Table 1 outlines the temperature and humidity limits for AIMM module operation.

Table 1. AIMM Temperature, Humidity, and Barometric Pressure Requirements

Operating Temperature	0° C to +65° C ambient
Operating Humidity	10% to 90% relative humidity
Storage Temperature	-50° C to +100° C
Storage Humidity	5% to 95% without condensation
Barometric Pressure (operating and storage)	105 kPa to 69 kPa (up to 9,850 feet)

Safety – UL Rating

Printed circuit board to have flammability rating of 94V-O. Markings to include UL tractability requirements per **UL Recognized Component Directory.**

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3. SDRAM Component Requirements

The SDRAM components populating the AIMM must meet the *Intel PC SGRAM/SDRAM Specification for Graphics* Version 0.99 requirements for 133 MHz parts. All AIMM SDRAM components must meet at minimum 133 MHz 3-3-3 timings. Modules must have the speed of the components labeled as specified in Section 8, *Labeling*.

The AIMM module consists of SDRAM components that make up 4 MB of local video memory. The 2Mx32 design contains an extra 4 MB of memory, for a total of 8 MB. Note that only 4 MB of the 2Mx32 based AIMM design are addressable.

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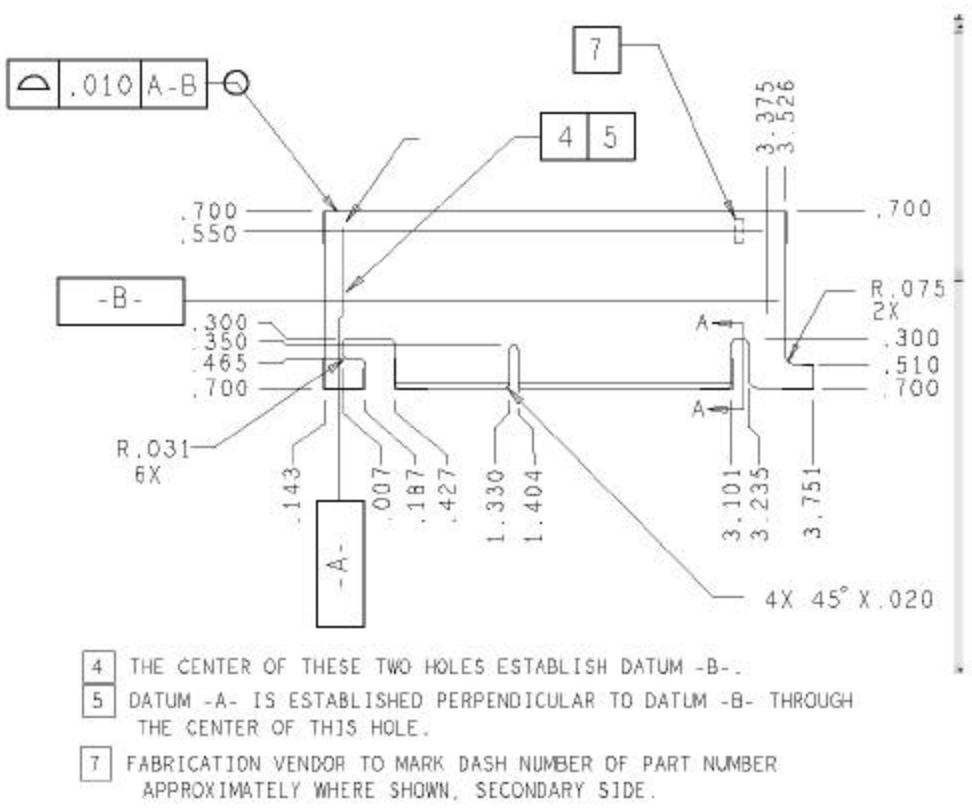
4. Mechanical Design

Figure 1. AIMM Outline Mechanical Drawing



Note: All dimensions are in inches. Tolerances are ± 0.005 inches.

The area below 400 mils is a component keepout zone. Do not place components within 400 mils of the bottom edge of the AIMM card.

Refer to the *Accelerated Graphics Port Interface Specification* for details of the card edge finger layout. The specification is located at the URL listed in the *Introduction Section*.

Note especially the edge bevel requirement in the *Accelerated Graphics Port Interface Specification.*

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5. Module Pinout

The following table contains the AIMM pinout. Note that the pin number designations refer to the corresponding pin locations in the AGP 3.3 volt and universal connectors.

Table 2. AIMM Pinout

Pin #	B	A	Pin #	B	A	Pin #	B	A
1	—	—	23	KEYWAY	KEYWAY	45	Vcc	Vcc
2	—	TYPEDET	24	KEYWAY	KEYWAY	46	DQ11	A7
3	—	—	25	KEYWAY	KEYWAY	47	Vddq	CS#
4	—	—	26	DQ21	TCLK0	48	—	—
5	GND	GND	27	DQ20	TCLK1	49	GND	GND
6	—	—	28	Vcc	Vcc	50	—	A6
7	—	—	29	DQ19	CAS#	51	DQ10	A1
8	DQ27	—	30	DQ18	—	52	Vddq	Vddq
9	Vcc	Vcc	31	GND	GND	53	DQ9	A5
10	DQ28	DQM3	32	—	—	54	DQ8	A2
11	DQ29	—	33	DQ17	RAS#	55	GND	GND
12	DQ30	DQ24	34	Vddq	Vddq	56	DQM1	A4
13	GND	GND	35	DQ16	A0	57	DQ0	A3
14	—	—	36	DQ15	A9	58	Vddq	Vddq
15	DQ31	DQ25	37	GND	GND	59	—	—
16	Vcc	Vcc	38	DQ14	A11	60	DQ1	DQ5
17	DQM2	DQ26	39	DQ13	A8	61	GND	GND
18	—	—	40	Vddq	Vddq	62	DQ2	DQ6
19	GND	GND	41	DQ12	A10	63	DQ3	DQ7
20	DQ23	WE#	42	—	—	64	Vddq	Vddq
21	DQ22	FSEL	43	GND	GND	65	DQ4	DQM0
22	KEYWAY	KEYWAY	44	—	—	66	—	—

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6. Bill Of Materials

Table 3. 1Mx16 AIMM Bill Of Materials

Item	Qty	Component Type	Value	Part No.	Reference	Package
1	19	Capacitor	27 pF	Kemet C0603C270K8GACor equivalent	C1, C2, C3, C4, C6, C7, C8, C9, C10, C11, C12, C13, C15, C16, C17, C18, C19, C20, C21	0603
2	2	SDRAM	1Mx16 2bank 133 MHz		U1, U2	TSOP50

NOTES: C5 and C14 are no-pop multi-land-pattern sites for 22 uF bulk decoupling capacitors. Current recommendation is to leave these pads unpopulated. Refer to the *Reference Schematics and Layout Section* for details.

Table 4. 2Mx32 AIMM Bill Of Materials

Item	Qty	Component Type	Value	Part No.	Reference	Package
1	17	Capacitor	27 pF	Kemet C0603C270K8GAC or equivalent	C1, C2, C3, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19	0603
2	1	SDRAM	2Mx32 4bank 133 MHz		U1	TSOP86

NOTES: C5 and C4 are no-pop multi-land-pattern sites for 22 uF bulk decoupling capacitors. Current recommendation is to leave these pads unpopulated. Refer to the *Reference Schematics and Layout Section* for details.

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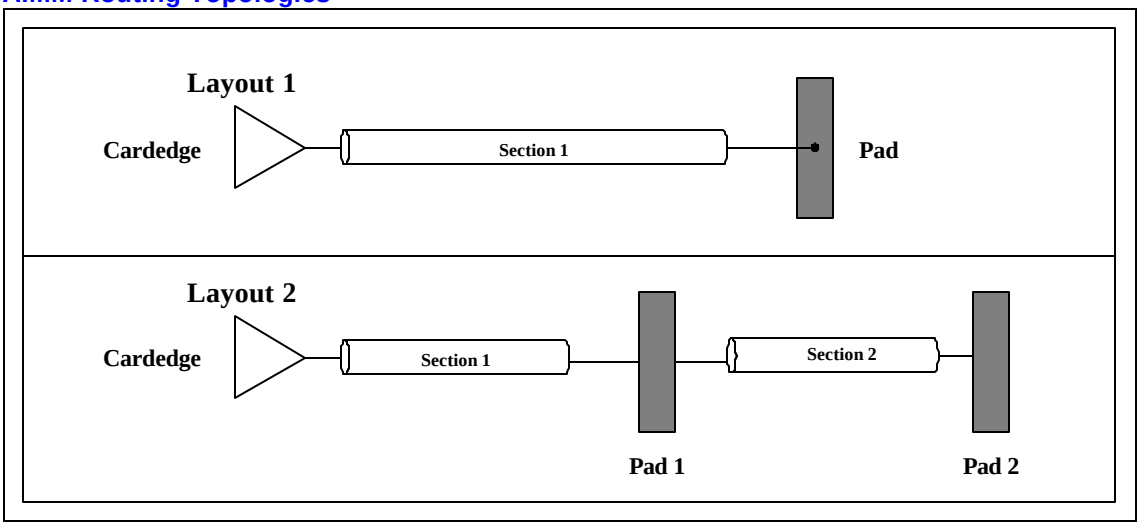
7. Layout and Routing

Figure 2. AIMM Routing Topologies



All nets on the AIMM card can be routed in one of the two topologies above. Layout 1 describes point-to-point connections (e.g., data lines) where one pin on the card edge must connect to one pin on one memory device. Layout 2 describes daisy-chained routes (e.g., address or control lines) where one pin on the card edge must connect to pins on each of two memory devices.

The following guidelines are subject to change.

Table 5. Signal Topologies, Lengths, and Pitches

Signal	Topology	Trace (mils)		Section 1		Section 2		Notes
		Width	Spacing	Min	Max	Min	Max	
A[11:0], CS#, WE#, CAS#, RAS#	2	5	10	0.5”	1.5”	1”	1.5”	
CLK[1:0], DQ[31:0]	1	5	10	1”	2”			Match within 500 mils

NOTES: For 2Mx32 AIMM solutions, all lines will be topology 1 (point-to-point) lines, and should be routed in accordance with the CLK and DQ guidelines in the table.

Examples of component placement and routing solutions for 1Mx16 and 2Mx32 AIMM designs can be found in *Section 9 - Reference Schematics and Layout.*

Component land pads are subject to the manufacturer’s discretion. Modifying the reference gerber land pads presented here and in the reference gerber electronic package to improve manufacturability is allowed.

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8. Labeling

The printed circuit board is required to have the following labeling contained in etch or in silkscreen:

- Flammability indicator (refer to Section 2 of this document)
- The text: AIMM – REV #.# (where #.# is the revision of the AGP Inline Memory Module specification to which the AIMM is designed.) Example: AIMM-REV 1.0

The assembled AIMM is required to have the following labeling on a component or a sticker (supplier option):

- AIMM-X-abc Example: AIMM-133-333

  Where:
  - X is the clock speed of the AIMM (133 MHz)
  - a = CL value
  - b = Trcd value
  - c = Trp value

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9. Reference Schematics and Layout

The schematics and layout provided describe a prototype AIMM solution. The AIMMs presented have not been tested for compliance and are subject to change.

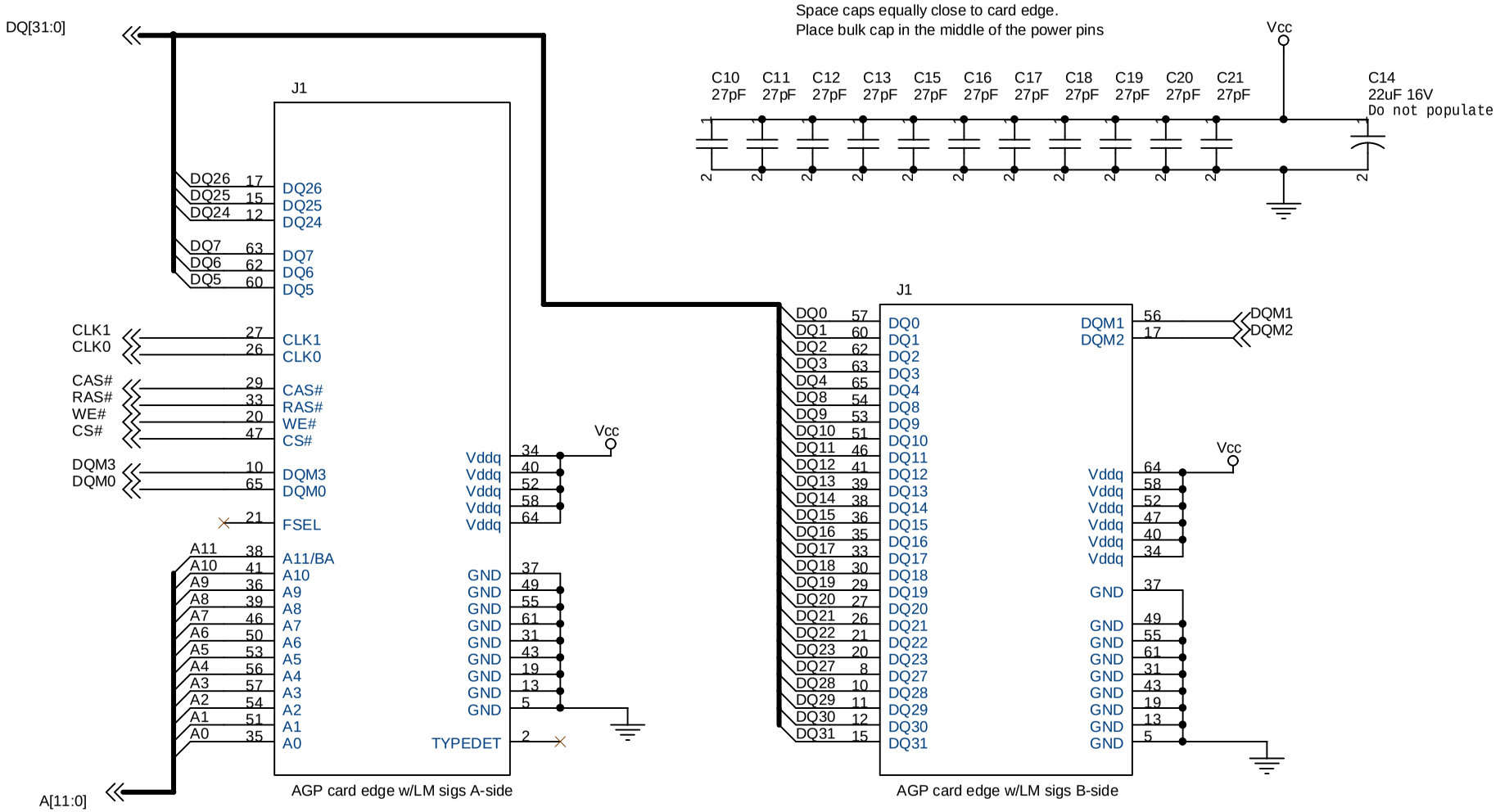
9.1. 1Mx16 Schematics

These schematics describe an AIMM that provides 4 MB of addressable SDRAM using 16 Mbit technology. Two 1Mx16 memory devices are used, arranged in a 1Mx32 configuration.

- **Sheet 1 – Card Edge** describes the connections at the AIMM card edge.
- **Sheet 2 – Memory Devices** describes the connections to the SDRAM devices on the AIMM card.

Note that the SDRAM components U1 and U2 must meet the *Intel PC SGRAM/SDRAM Specification for Graphics* Version 0.99 requirements for 133 MHz parts. AIMMs must be populated with SDRAM components meeting 3-3-3 timings.

C5 and C14 are sites for 22 uF bulk decoupling capacitors. This design leaves these sites unpopulated.



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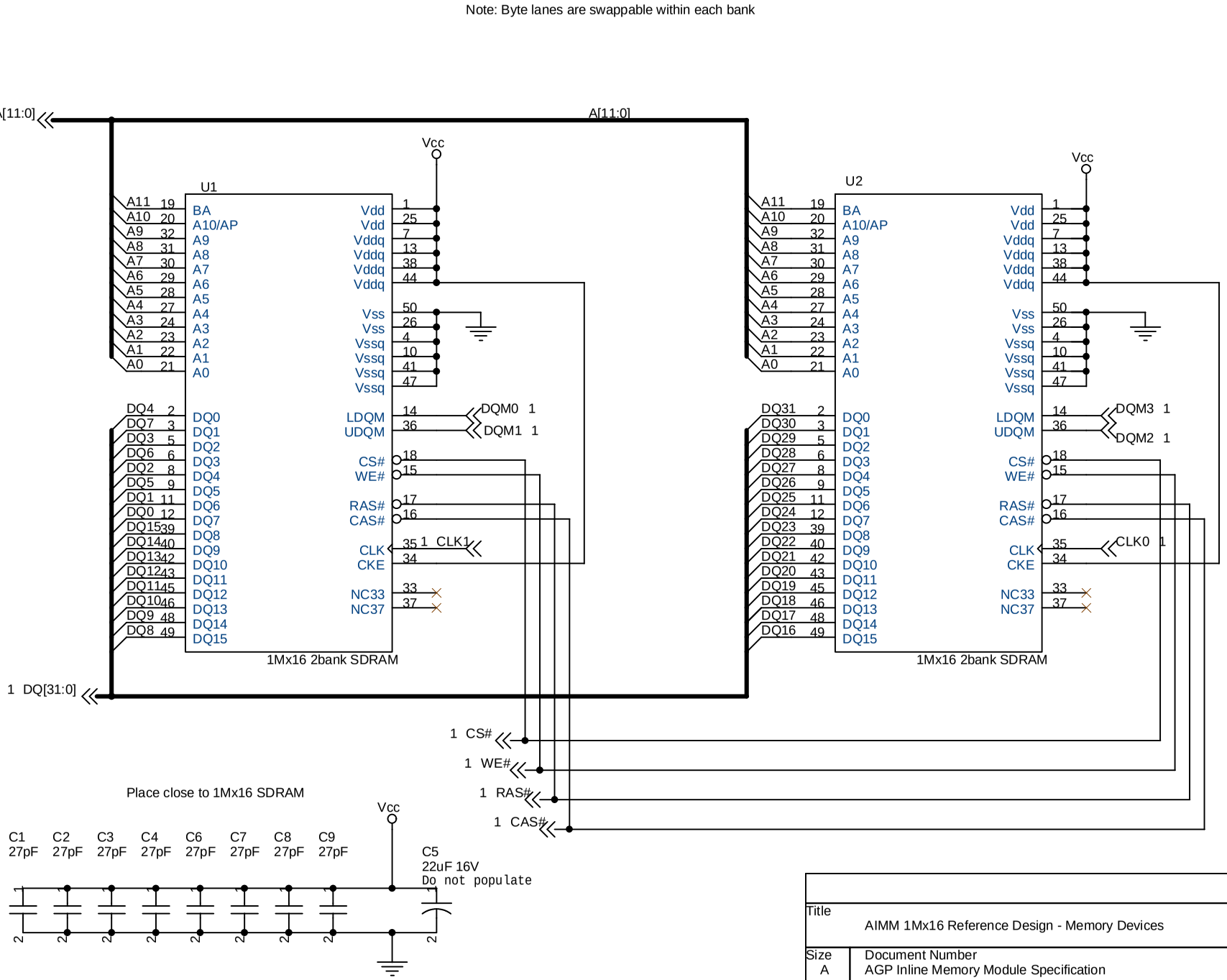
Size A	Document Number AGP Inline Memory Module Specification	Rev 1.0
Date: Wednesday, April 19, 2000	Sheet 1 of 2	

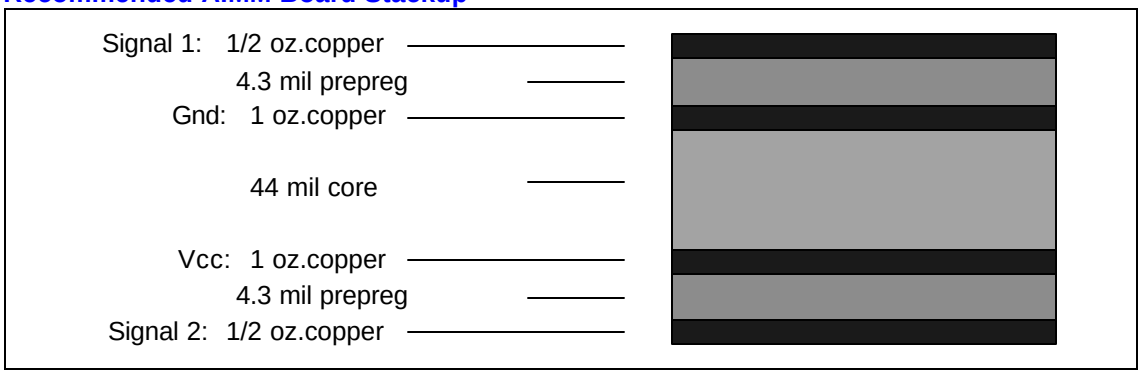


Title: AIMM 1Mx16 Reference Design - Memory Devices		
Size: A	Document Number: AGP Inline Memory Module Specification	Rev: 1.0
Date: Wednesday, April 19, 2000	Sheet 2 of 2	

9.2. 1Mx16 Routing and Stackup Example

All AIMMs are recommended to be designed on a single-sided assembly four-layer PCB. Nominal board thickness should be 62 mils. All traces are controlled impedance traces, specified at 60 ohms ±15%. The recommended stackup is below.

Figure 3. Recommended AIMM Board Stackup



Possible prepreg cloths are 2 ply 1080, 1 ply 1080 + 1 ply 106, or equivalents.

Figure 4 is a plot of the Signal 1 layer of a prototype AIMM (layer 1 of the stackup.) This is the component side of the AIMM board. Via capping is left to the discretion of the manufacturer.

Figure 5 is a plot of the Signal 2 layer of a prototype AIMM (layer 4 of the stackup). No components mount on this side of the AIMM board. Via capping is left to the discretion of the manufacturer.

Layers 2 and 3 are solid ground and power plane layers and are omitted from this document.

Component land pads are subject to the manufacturer's discretion. Modifying the reference gerber land pads presented here and in the reference gerber electronic package to improve manufacturability is allowed.

Figure 4. 1Mx16 Example Routing – Layer 1 – Component side

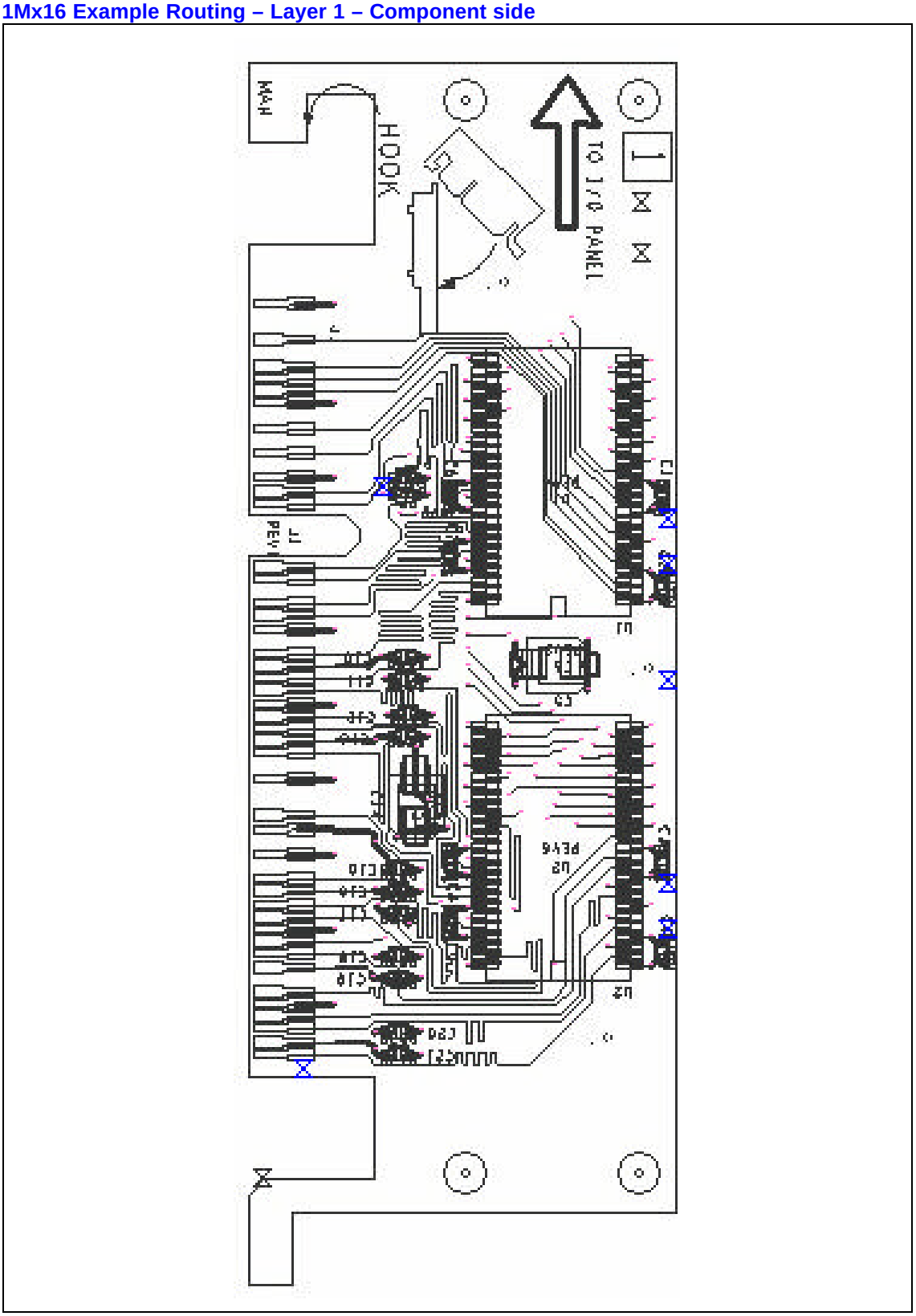
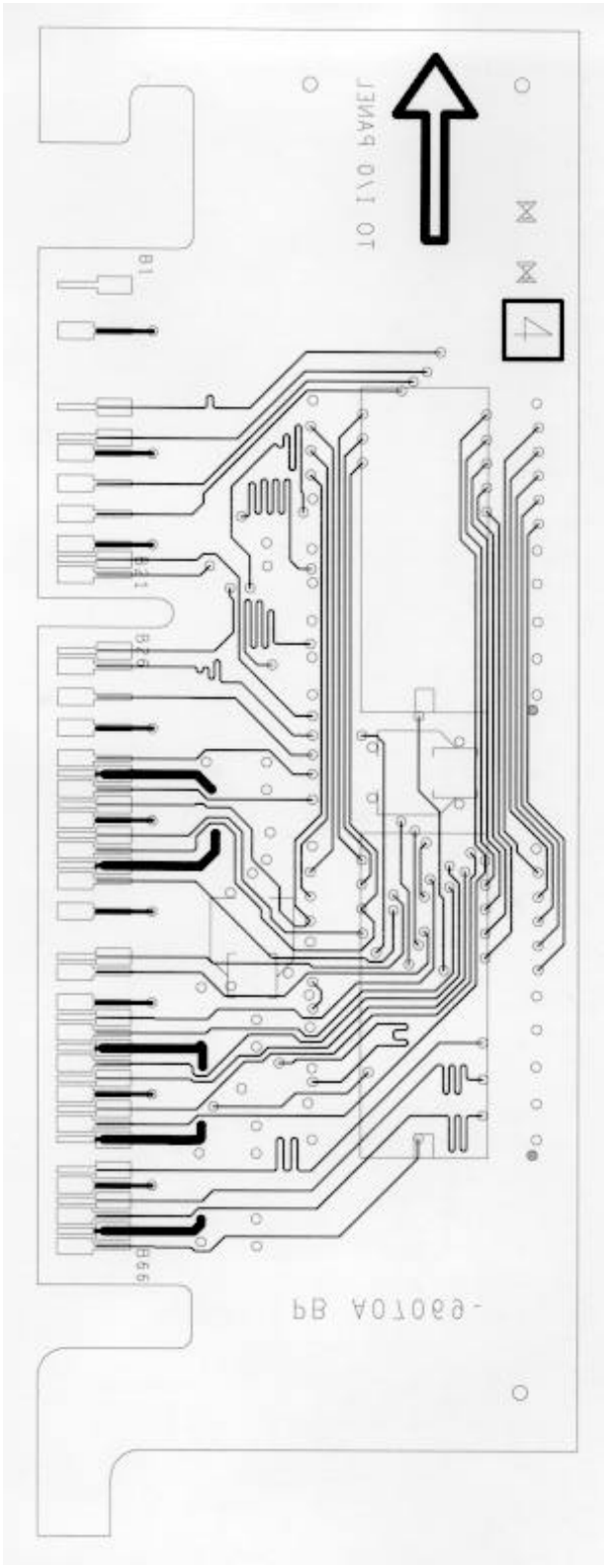


Figure 5. 1Mx16 Example Routing – Layer 4 – Solder side



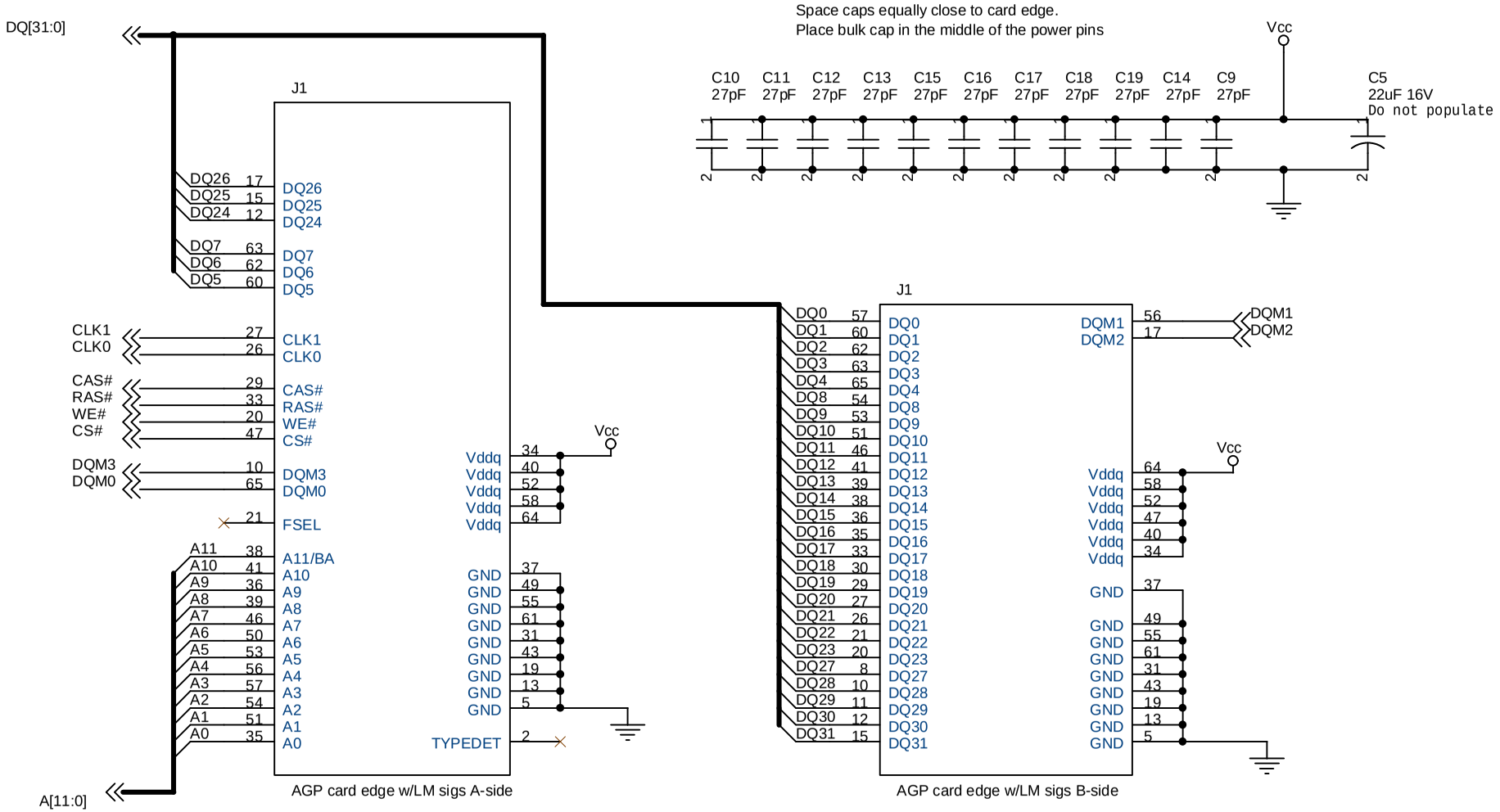
9.3. 2Mx32 Schematics

These schematics describe an AIMM that provides 4 MB of addressable SDRAM using 64 Mbit technology. One 2Mx32 memory device is used. Its upper bank-select address line is tied low to present a 1Mx32 SDRAM configuration.

- **Sheet 1 – Card Edge** describes the connections at the AIMM card edge.
- **Sheet 2 – Memory Device** describes the connections to the SDRAM device on the AIMM card. Note that either CLK0 or CLK1 can be used for the SDRAM clock. Using whichever clock is easier to route is recommended.

Note that the SDRAM components U1 and U2 must meet the *Intel PC SGRAM/SDRAM Specification for Graphics* Version 0.99 requirements for 133 MHz parts. SDRAM components must meet at a minimum 3-3-3 timings.

C4 and C5 are sites for 22 uF bulk decoupling capacitors. This design leaves these sites unpopulated.



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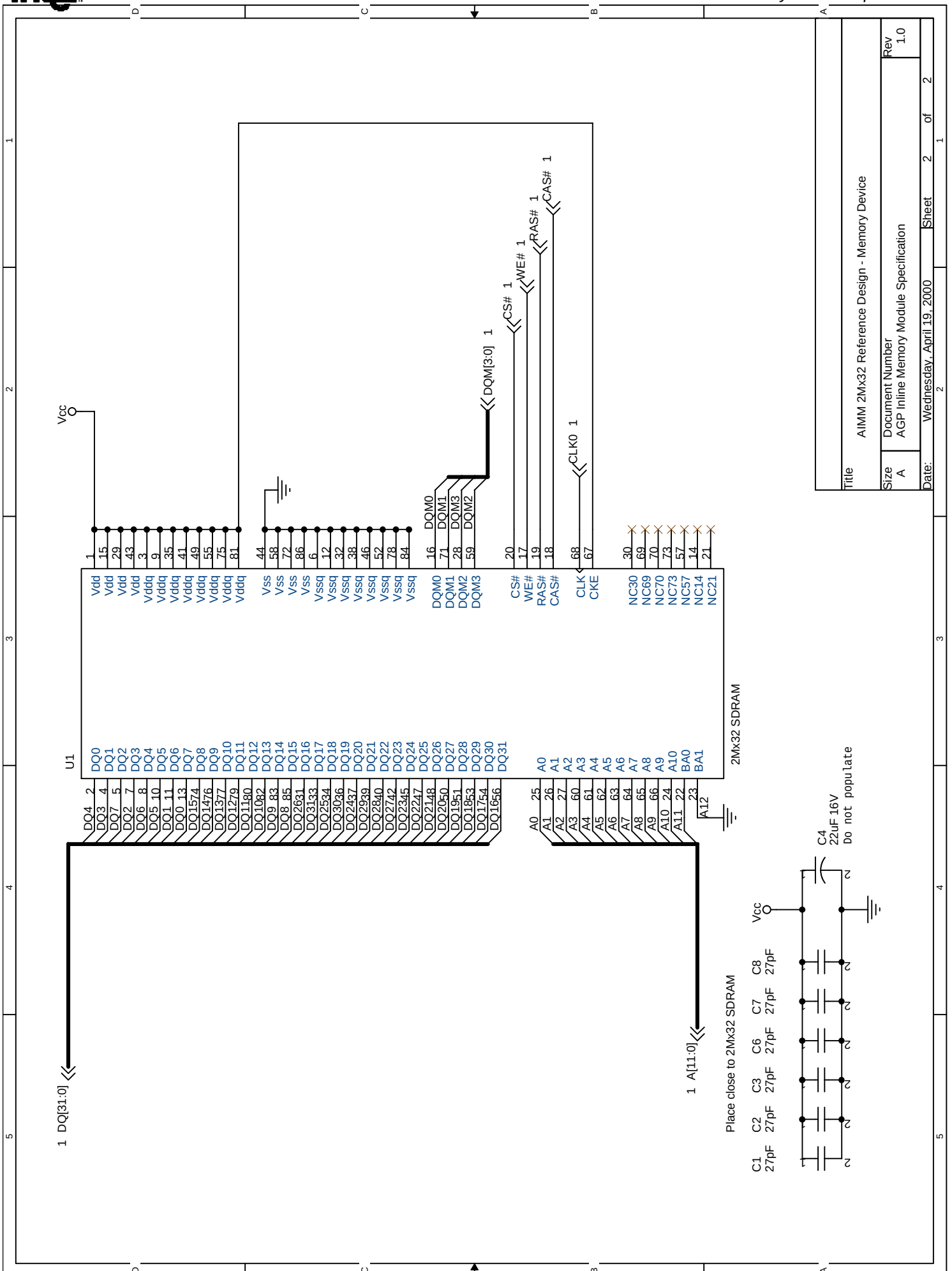
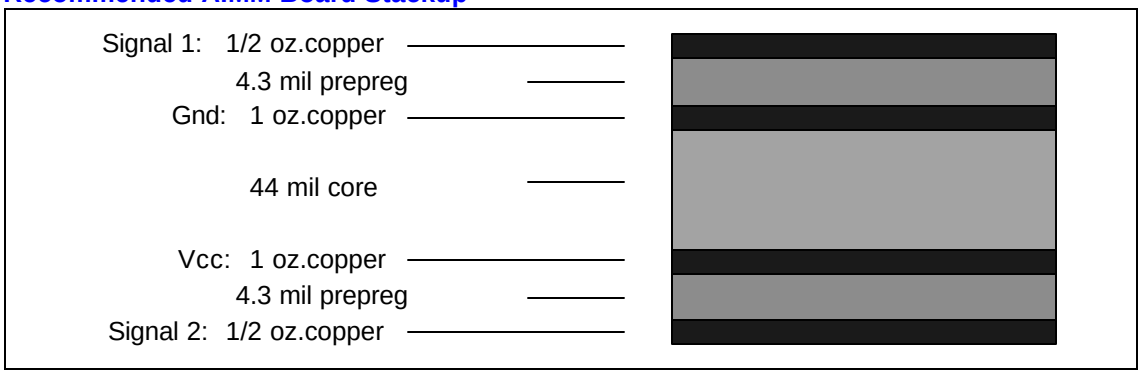
Size A	Document Number AGP Inline Memory Module Specification	Rev 1.0
Date: Wednesday, April 19, 2000	Sheet 1 of 2	


Title
AIMM 2Mx32 Reference Design - Memory Device
Size A
Document Number
AGP Inline Memory Module Specification
Rev 1.0
Date: Wednesday, April 19, 2000
Sheet 2 of 2
U1
2Mx32 SDRAM
Vcc
DQM[3:0] 1
CS# 1
WE# 1
RAS# 1
CAS# 1
CLK0 1
1 DQ[31:0]
1 A[11:0]
Place close to 2Mx32 SDRAM
C1 27pF
C2 27pF
C3 27pF
C6 27pF
C7 27pF
C8 27pF
C4 22uF 16V
Do not populate

9.4. 2Mx32 Routing and Stackup Example

All AIMMs are recommended to be designed on a single-sided assembly four-layer PCB. Nominal board thickness should be 62 mils. All traces are controlled impedance traces, specified at 60 ohms ±15%. The recommended stackup is shown below.

Figure 6. Recommended AIMM Board Stackup



Possible prepreg cloths are 2 ply 1080, 1 ply 1080 + 1 ply 106, or equivalents.

Figure 7 is a plot of the component-side signal layer of a prototype AIMM (layer 1 of the stackup.) This is the component side of the AIMM board. Via capping is left to the discretion of the manufacturer.

Figure 8 is a plot of the solder-side signal layer of a prototype AIMM (layer 4 of the stackup). No components are assembled on this side of the AIMM board. Via capping is left to the discretion of the manufacturer.

Layers 2 and 3 are solid ground and power plane layers, and are omitted from this document.

Component land pads are subject to the manufacturer's discretion. Modifying the reference gerber land pads presented here and in the reference gerber electronic package to improve manufacturability is allowed.

Figure 7. 2Mx32 Example Routing – Layer 1 – Component Side

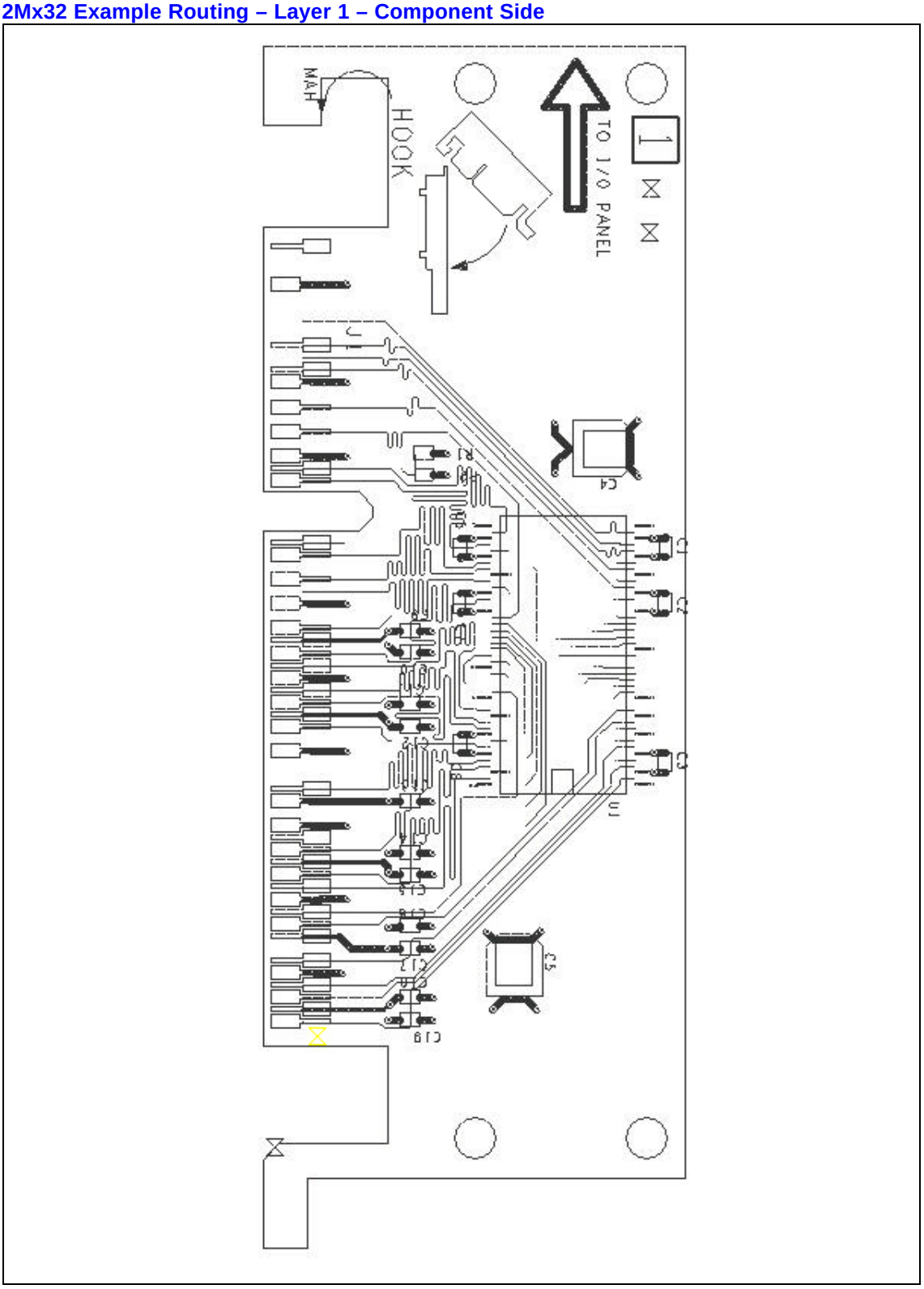


Figure 8. 2Mx32 Example Routing – Layer 4 – Solder side